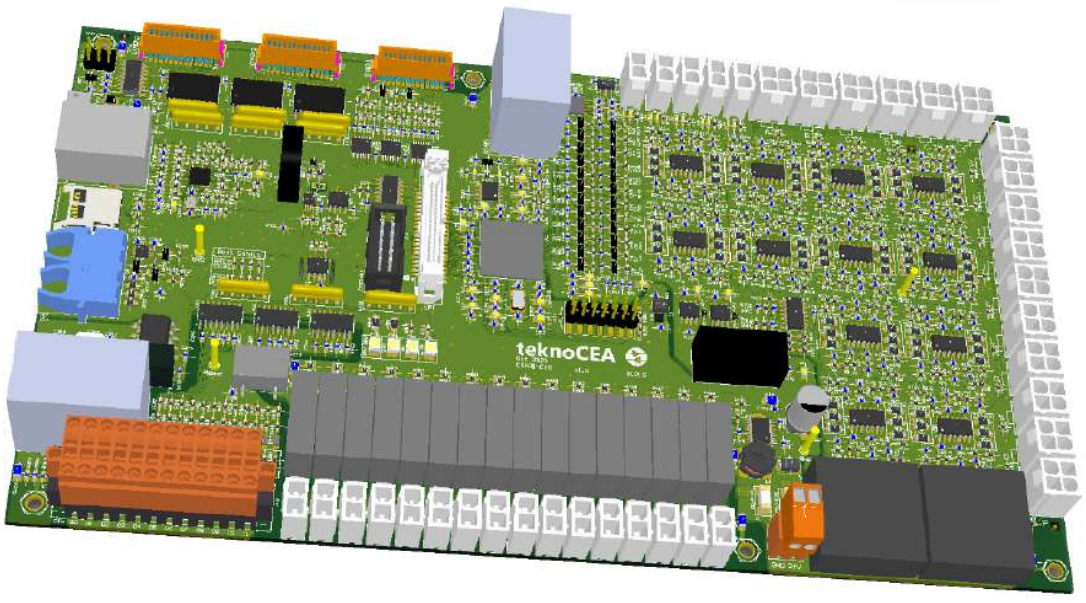
teknoCEA

CDA01-CU5 control board

CDA01-CU5 Technical Reference Manual

Rev. 1.0

February 2024



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Contents

1 Introduction to CDA01-CU5 **6**
1.1 Overview of the CDA01-CU5 . . . 6
1.2 Key features of the CDA01-CU5 . . . 6
1.2.1 Hardware features . . . 6
1.2.2 Software and programming tools . . . 8
1.3 Functional overview of the CDA01-CU5 . . . 9

2 Operation of the CDA01-CU5 **10**
2.1 General description . . . 10
2.2 Memory Map . . . 10
2.3 CDA01-CU5 connectors . . . 11
2.4 Boot sequence . . . 12
2.5 Power supplies . . . 12
2.6 JTAG . . . 13
2.7 ADC . . . 14
2.8 Temperature Inputs . . . 17
2.9 RS485 . . . 19
2.10 Power Converter Interface . . . 20
2.11 DAC . . . 24
2.12 μUSB-OTG . . . 25
2.13 Ethernet . . . 26
2.14 μSD . . . 27
2.15 Temperature protection environment, RTC & EEPROM . . . 28
2.16 Fiber optic synchronization (F. O. SYNC.) . . . 29
2.17 Isolated CAN . . . 30
2.18 Digital inputs . . . 31
2.19 Relay outputs . . . 32
2.20 Configuration by default of CDA01-CU5 . . . 33
2.20.1 Boot sequence . . . 33
2.20.2 ADC . . . 34
2.20.3 Digital input . . . 35
2.20.4 Fiber optic synchronization . . . 35
2.21 Security Precautions . . . 36
2.21.1 General precautions . . . 36
2.21.2 Earthing . . . 36

3 Layout **38**

4 Mechanical drawings **39**

Tecnologies de control de l'electricitat i automatització, S.L.
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List of Figures

1 Picture of a fully populated CDA01-CU5. 6
2 CDA01-CU5 block diagram. 9
3 CDA01-CU5 layout 10
4 CDA01-CU5 connectors. 11
5 Boot configuration resistors. 12
6 ADC's circuit. 14
7 J40-J55 connector, pin arrangement 17
8 Temperature input schematics 17
9 Temperature input multiplexer schematics 18
10 RS-485 schematics 19
11 Power converter interface block diagram 21
12 DAC connection 25
13 DAC connector J21 layout 25
14 Micro SD card schematics 27
15 I2C communications schematics 28
16 Fiber optic configuration schematics 29
17 Flip-flop circuit schematics 30
18 CAN circuit schematics 30
19 Digital inputs schematics 32
20 Relay outputs schematics 33
21 Boot configuration resistors by default. 34
22 CDA01-CU5 Layout. 38
23 CDA01-CU5 Mechanical drawings. 39

List of Tables

1 Function of connectors. 11
2 Boot configurations. 12
3 J11 connector, 24 V power supply, pin function and arrangement. 13
4 J12 connector, JTAG interface, pin function and arrangement. 13
5 ADC's location on CDA01-CU5. 15
6 ADC's configurations. 16
7 J40-J55 connector, pin function. 16
8 Multiplexer selector configuration 18
9 RS485, ST3485 transceiver pins 19
10 J6 connector, RS485 pin-out. 19
11 J71 connector, digital I/O interface, pin function and arrangement. 22
12 J72 connector, digital I/O interface, pin function and arrangement. 23
13 J73 connector, digital I/O interface, pin function and arrangement. 24
14 SPI communication pins 25
15 DAC connector J21 pin function and arrangement. 25
16 J15 connector pin function and arrangement. 26
17 LAN8710A, concerto microcontroller pins. 26
18 Ethernet connector J16 pin function and arrangement 27
19 SSI communication pins 27

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20 SD connector J14 pin function and arrangement 28
21 I2C communication pins 28
22 Flip flop logic table. 30
23 CAN connector J5 pin function and arrangement 31
24 CAN communication pins 31
25 Digital inputs pin configuration and arrangement 32
26 Relay output connectors. J1-J4, J7, J9, J17, J18, J20, J22-J28 links to Concerto pins . . 33
27 ADC's configuration by default. 34

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About This Manual

This document describes board-level operations of the CDA01-CU5 based on the Texas Instruments F28M36P63C2 Concerto family digital microcontroller (DSP). This TI microcontroller family is a multi-core system-on-chip microcontroller unit (MCU) with independent communication and real-time control subsystems.

The CDA01-CU5 is a stand-alone module, allowing engineers and software developers the evaluation of certain characteristics of the F28M36P63C2 Concerto to determine processor applicability to the design requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Information About Cautions

This book may contain cautions.

> **IMPORTANT NOTICE**
> **This is an example of caution**

A caution statement describes a situation that could potentially damage your hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments F28M36x Technical Reference Manual, literature #spruhe8e.pdf
Texas Instruments F28M36P63C2 datasheet, literature #f28m36p63c2.pdf

1 Introduction to CDA01-CU5

This chapter provides a description of the CDA01-CU5 control board based on F28M36P63C2 Concerto, key features, and block diagram of the circuit board.

1.1 Overview of the CDA01-CU5

The CDA01-CU5 is a stand-alone control card based on the Texas Instruments F28M36P63C2 Concerto microcontroller. The control board includes all the needed peripherals and circuits for a complete power electronics product or project, including communications capabilities. Figure 1 shows a picture of the fully populated board.
The control board includes 3 control connectors, each fully compatible with one teknoCEA power converter stack.

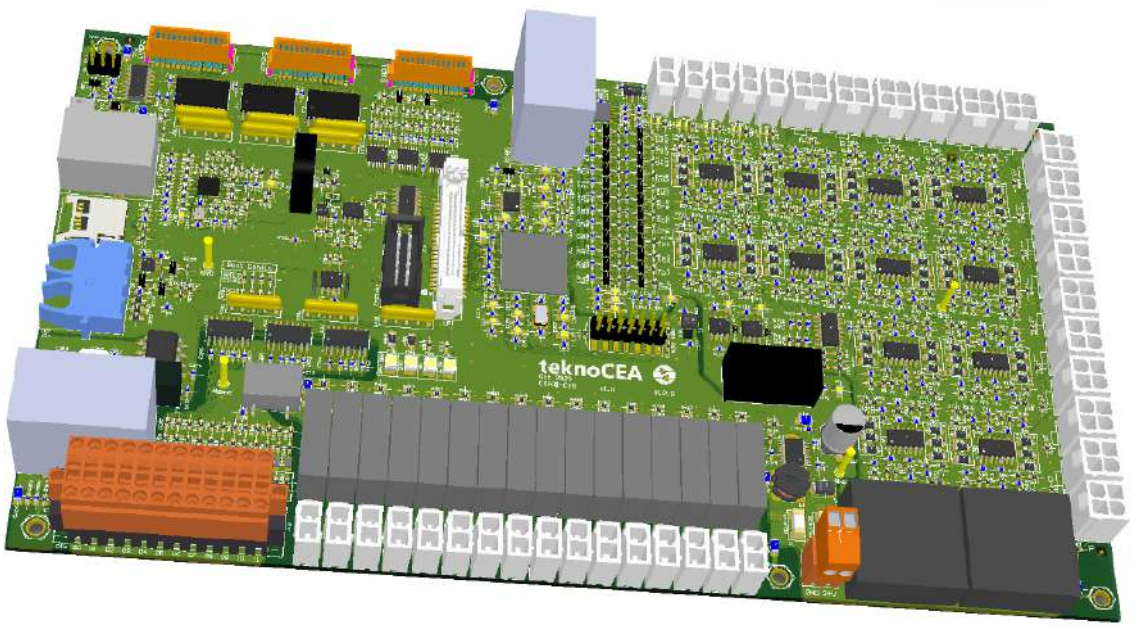


Figure 1: Picture of a fully populated CDA01-CU5.

The CDA01-CU5 is based on the F28M36P63C2 Concerto microcontroller. The CDA01-CU5 allows full speed implementation of F28M36P63C2 Concerto code. The platform also implements several circuits and connectors to use peripherals of the microcontroller.

An on-board JTAG connector provides the interface to emulators and C2000 Code Composer Studio™ programming and debugging tool from Texas Instruments. It can be downloaded from TI web page.

1.2 Key features of the CDA01-CU5

1.2.1 Hardware features

The CDA01-CU5 has the following features:

- F28M36P63C2 Concerto

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  - Master Subsystem – ARM Cortex – M3
    - Up to 125 MHz
    - 1 MB of Flash (ECC)
    - 128 kB of RAM (ECC or Parity)
    - 64 kB of Shared RAM
    - 2 kB of IPC Message RAM
  - Control Subsystem TMS320C28x 32-Bit CPU
    - Up to 150 Mhz
    - C28x Core Hardware Built-in Self-Test
    - Embedded Memory
      - 512 kB of Flash (ECC)
      - 36 kB of RAM (ECC or Parity)
      - 64 kB of Shared RAM
      - 2 kB of IPC Message RAM
  - 20 MHz input clock
- 12 bit Analog to Digital converter (ADC) with 24 input channels
  - 16 general inputs from J40 to J55 connectors
  - 3 inputs in J71 flat connector
  - 2 inputs in J72 flat connector
  - 2 inputs in J73 flat connector
  - 1 input for 8 temperatures sensors routed through a multiplexer
    - 5 specific inputs from J31 to J35 connectors
    - 1 input in J71 flat connector
    - 1 input in J72 flat connector
    - 1 input in J73 flat connector
- 16 digital outputs
- 18 PWM signals with 9 driver FAULTs and Reset pin + 1 PWM fan signal
  - 6 PWM outputs in J71 flat connector
  - 6 PWM outputs in J72 flat connector
  - 6 PWM outputs in J73 flat connector
  - 3 driver FAULT inputs in J71 flat connector
  - 3 driver FAULT inputs in J72 flat connector

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  - 3 driver FAULT inputs in J73 flat connector
  - 3 PWM outputs in J71 flat connector
  - 3 PWM outputs in J72 flat connector
  - 3 PWM outputs in J73 flat connector
  - 1 PWM fan output shared in J71, J72 and J73 connectors
- Fiber optics transmitter and receiver connectors for PWM synchronization
- On board isolated CAN 2.0 interface with transceiver and duplicated RJ45 connector for daisy chain
- On board RS-485 with transceiver and duplicated RJ45 connector for daisy chain
- On board Ethernet connector 10/100 ENET 1588 MII with transceiver
- On board Universal Serial Bus On-the-Go (USB-OTG) with transceiver and micro USB connector
- On board microSD Push-Push Card Connector
- 12 isolated digital inputs in J19 flat connector
- 16 general purpose relay output
- Digital to Analog converter (DAC) with 4 output channels wired to a 6 pin connector
- On board 256 kB external EEPROM memory with I2C interface
- On board Real Time Clock (RTC) with I2C interface
- On board IEEE 1149.1 JTAG emulation connector
- Unique 24 VDC power supply input

1.2.2 Software and programming tools

- Texas Instruments controlSUITE™Software Suite: Software and Development Tools for C2000™ Microcontrollers
- Texas Instruments F021 Flash Application Programming Interface
- Texas Instruments F28M36x Concerto™ MCUs Silicon Errata (Silicon Revisions F, E, B, A, 0)
- Texas Instruments C2000 Real-Time Control MCU Peripherals
- TI F28xx Code Composer Studio™ Integrated Development Environment.
- Texas Instruments F28M36x Peripheral Driver Library
- teknoCEA CDA03-JTAG2

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1.3 Functional overview of the CDA01-CU5

Figure 2 shows a block diagram of the basic configuration for the CDA01-CU5. This figure shows the microcontroller and all the peripheral devices connected to it.

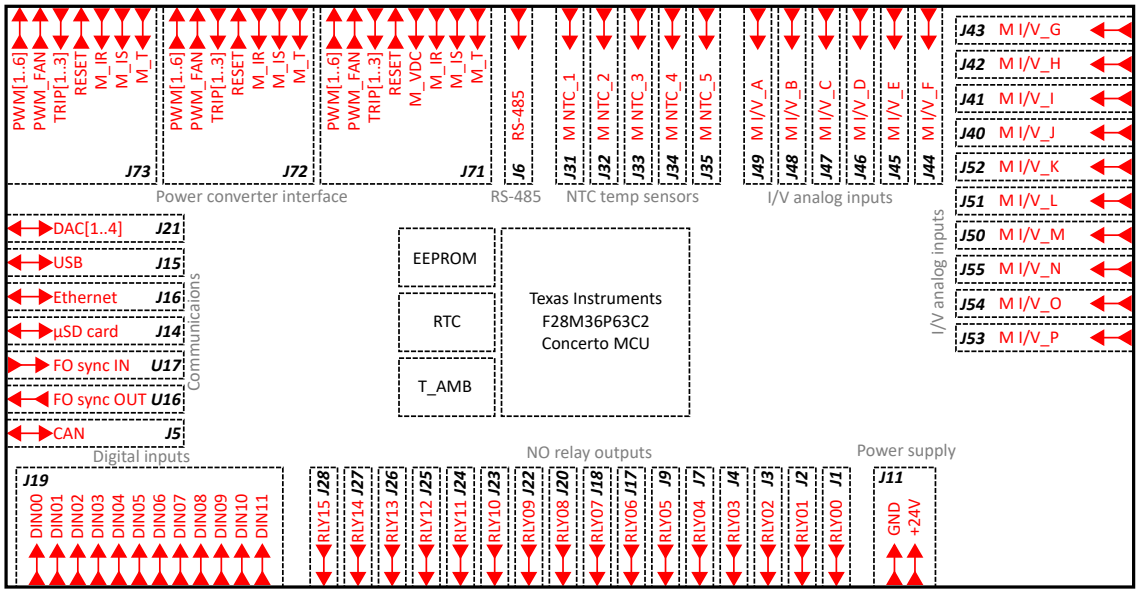


Figure 2: CDA01-CU5 block diagram.

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2 Operation of the CDA01-CU5

2.1 General description

The CDA01-CU5 is a 140 mm x 250 mm, 6 layered printed circuit board, powered by a unique external 24 VDC power supply. Figure 3 shows the layout of the top side of CDA01-CU5.

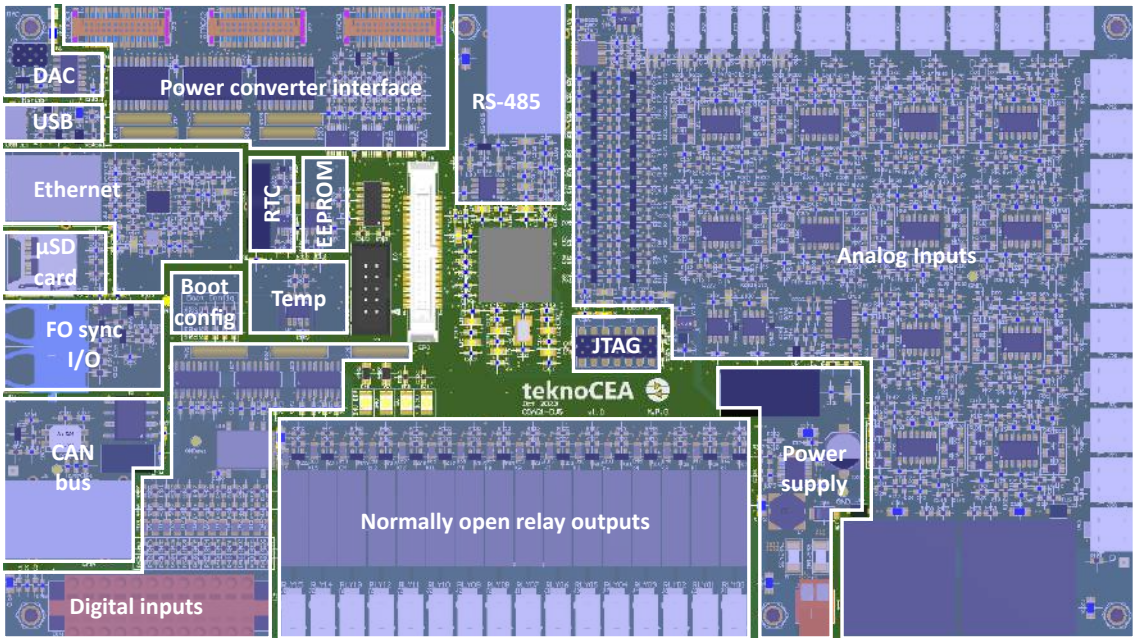


Figure 3: CDA01-CU5 layout

2.2 Memory Map

The CDA01-CU5 includes the following on-chip memory:

- Master Subsystem – ARM Cortex – M3
  - 1 MB of Flash (ECC)
  - 128 kB of RAM (ECC or Parity)
  - 64 kB of Shared RAM
  - 2 kB of IPC Message RAM
- C28x Core memory
  - 512 kB of Flash (ECC)
  - 36 kB of RAM (ECC or parity)
  - 64 kB of Shared RAM
  - 2 kB of IPC Message RAM

In addition, an $8 \times 32kB$ serial EEPROM is provided on board. The external memory is managed through an I2C bus communication.

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Please, refer to F28M36x literature for further information on memory map.

2.3 CDA01-CU5 connectors

The CDA01-CU5 has fifty-two connectors that are shown in Figure 4. The function of each connector is shown in the Table 1.

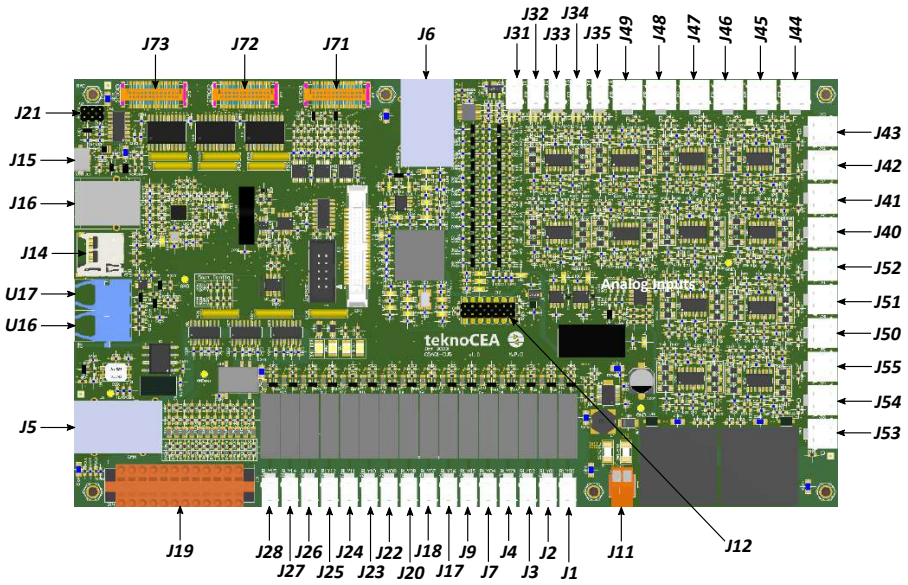


Figure 4: CDA01-CU5 connectors.

Connector	Function
J1-J4, J7, J9, J17, J18, J20, J22-J28	Relay Outputs
J5	CAN
J6	RS485
J11	24 V power supply
J12	JTAG
J14	micro-SD
J15	micro-USB-OTG
J16	Ethernet
J19	Isolated Digital Inputs
J21	DAC Outputs
J31-J35	Temperature Inputs
J40-J55	ADC inputs
J71, J72, J73	Stack Outputs
U16	PWM SYNC OUT fiber optic
U17	PWM SYNC IN fiber optic

Table 1: Function of connectors.

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2.4 Boot sequence

Boot sequence is used to configure the Master Subsystem and the Control Subsystem for execution of application code.

Figure 5 shows the configuration resistors matrix and Table 2 describes the main configurations. More options can be found in Texas Instruments F28M36x Technical Reference Manual.

Boot Mode	GPIO34	GPIO35	GPIO47	GPIO43
Boot from Parallel GPIO	0 R331	0 R332	0 R333	0 R334
Boot to Master Subsystem RAM	0 R331	0 R332	0 R333	1 R330
Boot from Master Subsystem Serial Peripherals (UART0/SSI0/I2C0)	0 R331	0 R332	1 R329	0 R334
Boot from Master Subsystem CAN interface	0 R331	0 R332	1 R329	1 R330
Boot from Master Subsystem Ethernet interface	1 R327	1 R328	0 R333	0 R334
Boot to Master Subsystem Flash memory	1 R327	1 R328	1 R329	1 R330

Table 2: Boot configurations.

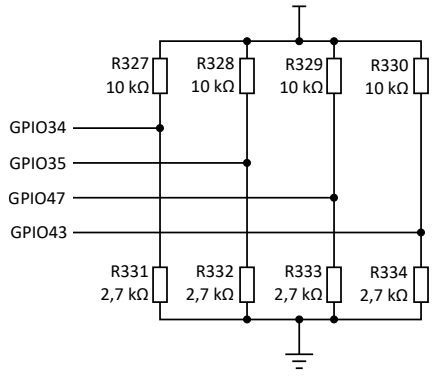


Figure 5: Boot configuration resistors.

IMPORTANT NOTICE
Only one of two resistors, 3,3 V 10 kΩ or GND 2,7 kΩ of each GPIO must be soldered.

2.5 Power supplies

The CDA1-CU5 must be powered by a unique external 24 V power supply. The additional needed voltages of ±15 V, ±12 V, 5 V, 3,3 V and 1,65 V are generated internally and all of them are referenced to the same ground (GND). 5 V and 3 V are generated by LM3100 and TPS62291 step down converters

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respectively from Texas Instruments. However, ±12 V are generated by TMR 3-2423 step down converter from Traco Power plus TPS78L12 and TPS79L12 from Taiwan Semiconductors. Additional ±15 V are provided to the board for supplying the Voltage/Current sensors by using two SKM30F isolated converters from Mean Well. Finally, 1,65 V are generated by TS431 low voltage adjustable shunt reference from STMicroelectronics plus a OPA4277 operational amplifier from TI as buffer and filter.

Three LEDs (D63 for 24 V D30 for 5 V and D31 for 3,3 V) indicate the status of these power supplies. Additionally, LED D45 indicates if the isolated digital inputs are supplied from the onboard isolated power supply. The total power consumption from the 24 V external power supply can be up to 240 W depending on voltage/current sensor and power stacks consumption. The 10 A fuse F1 protects the 24 V input supply from an overload situation.

The J11 connector has a 2x1 pin arrangement and is used to supply CDA01-CU5. The J11 connector is from Weidmuller, manufacturer reference SL 3.5/2/180G. The female connector that matches the J12 is also from Weidmuller, reference BL 3.5/2. Pin arrangement and function of connector J11 is summarized in Table 3.

Pin	Pin name	Function	Description
1	+24 V	Power	Power supply +24 V_{DC}
2	GND	Power	Ground for power supply

Table 3: J11 connector, 24 V power supply, pin function and arrangement.

2.6 JTAG

A JTAG connector is available for configuration. J12 connector is from TE Connectivity, manufacturer reference 1241050-7.

The pin-out of J12, which includes the JTAG signals, is shown in Table 4.

Pin	Pin name
1	TMS
2	TRST
3	TDI
4	GND
5	TPD (3,3 V)
6	No pin
7	TDO
8	GND
9	TCK
10	GND
11	TCK
12	GND
13	EMU0
14	EMU1

Table 4: J12 connector, JTAG interface, pin function and arrangement.

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IMPORTANT NOTICE
The F28M36P63C2 Concerto supports 3,3 V Input/Output levels, which are NOT 5 V tolerant. Connecting the CDA01-CU5 to a system with 5 V Input/Output levels will damage the F28M36P63C2.

2.7 ADC

Each ADC channel consists of 2 analog input stages. The first analog input stage consists of a pull-down resistor (in order not to saturate ADC input when no voltage is connected) for voltage input signal or a shunt resistor for current input signal. An analog voltage follower circuit is used to provide a high impedance input to the pull-down/shunt resistors.

The second stage is a second order filter with offset and gain. Changing the resistors and capacitors values, user can configure the input voltage range (10 V or 5 V), unipolar o bipolar ADC (±5 V or ±10 V) and if the sum stage is a second or a first order filter. Figure 6 shows the schematic of ADC channel and Table 5 and Table 6 how to configure all possible options.

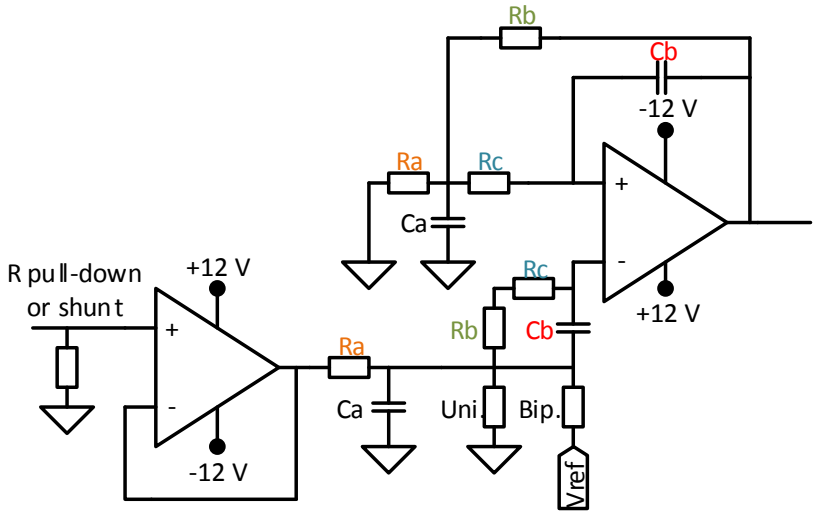


Figure 6: ADC's circuit.

IMPORTANT NOTICE
Only one of the bipolar or unipolar resistors can be soldered!
Be aware of power shunt resistor dissipation. The default configuration is specified in Chapter 2.20.2.
Cut-off frequency is 5 kHz!

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Connector	Input	ADC	Type	Polarity	Ra	Rb	Rc	Ca	Cb
J50	M	ADC1.A0	Shunt/Pull-down R9 R10 R11 / R311	Uni/Bipolar R21 / R22	R3 R12	R1 R19	R4 R13	C3 C10	C1 C9
J71	Stack 1 Ir	ADC1.A2	Shunt/Pull-down R14 R15 R16 / -	Uni/Bipolar R23 / R24	R5 R17	R2 R20	R6 R18	C4 C12	C2 C11
J72	Stack 2 Ir	ADC1.A3	Shunt/Pull-down R33 R34 R35 / -	Uni/Bipolar R45 / R46	R27 R36	R25 R43	R28 R37	C15 C22	C13 C21
J51	L	ADC1.A4	Shunt/Pull-down R38 R39 R40 / R312	Uni/Bipolar R47 / R48	R29 R41	R26 R44	R30 R42	C16 C24	C14 C23
J73	Stack 3 Ir	ADC1.A6	Shunt/Pull-down R62 R63 R64 / -	Uni/Bipolar R71 / R72	R53 R66	R50 R68	R54 R65	C28 C35	C26 C34
J52	K	ADC1.A7	Shunt/Pull-down R57 R58 R59 / R432	Uni/Bipolar R69 / R70	R52 R61	R49 R67	R51 R60	C27 C36	C25 C33
J55	N	ADC1.B0	Shunt/Pull-down R86 R87 R88 / R476	Uni/Bipolar R95 / R96	R77 R90	R74 R92	R78 R89	C40 C47	C38 C46
J71	Stack 1 Is	ADC1.B2	Shunt/Pull-down R81 R82 R83 / -	Uni/Bipolar R93 / R94	R76 R85	R73 R91	R75 R84	C39 C48	C37 C45
J72	Stack 2 Is	ADC1.B3	Shunt/Pull-down R110 R111 R112 / -	Uni/Bipolar R119 / R120	R101 R114	R98 R116	R102 R113	C52 C59	C50 C58
J54	O	ADC1.B4	Shunt/Pull-down R105 R106 R107 / R478	Uni/Bipolar R117 / R118	R100 R109	R97 R115	R99 R108	C51 C60	C49 C57
J73	Stack 3 Is	ADC1.B6	Shunt/Pull-down R134 R135 R136 / -	Uni/Bipolar R143 / R144	R125 R138	R122 R140	R126 R137	C64 C71	C62 C70
J53	P	ADC1.B7	Shunt/Pull-down R129 R130 R131 / R480	Uni/Bipolar R141 / R142	R124 R133	R121 R139	R123 R132	C63 C72	C61 C69
J40	J	ADC2.A0	Shunt/Pull-down R158 R159 R160 / R481	Uni/Bipolar R167 / R168	R149 R162	R146 R164	R150 R161	C76 C83	C74 C82
J41	I	ADC2.A2	Shunt/Pull-down R153 R154 R155 / R487	Uni/Bipolar R165 / R166	R148 R157	R145 R163	R147 R156	C75 C84	C73 C81
J42	H	ADC2.A3	Shunt/Pull-down R182 R183 R184 / R510	Uni/Bipolar R191 / R192	R173 R186	R170 R188	R174 R185	C88 C95	C86 C94
J43	G	ADC2.A4	Shunt/Pull-down R177 R178 R179 / R488	Uni/Bipolar R189 / R190	R172 R181	R169 R187	R171 R180	C87 C96	C85 C93
J44	F	ADC2.A6	Shunt/Pull-down R206 R207 R208 / R511	Uni/Bipolar R215 / R216	R197 R210	R194 R212	R198 R209	C100 C107	C98 C106
J45	E	ADC2.A7	Shunt/Pull-down R201 R202 R203 / R512	Uni/Bipolar R213 / R214	R196 R205	R195 R211	R193 R204	C99 C108	C97 C105
J49	A	ADC2.B2	Shunt/Pull-down R230 R231 R232 / R513	Uni/Bipolar R239 / R240	R221 R234	R218 R236	R222 R233	C112 C119	C110 C118
-	Temp[1..8]	ADC2.B0	Shunt/Pull-down R225 R226 R227 / -	Uni/Bipolar R237 / R238	R220 R229	R217 R235	R219 R228	C111 C120	C109 C117
J48	B	ADC2.B3	Shunt/Pull-down R249 R250 R251 / R516	Uni/Bipolar R261 / R262	R244 R253	R241 R259	R243 R252	C123 C132	C121 C129
J71	Stack 1 V_{DC}	ADC2.B4	Shunt/Pull-down R254 R255 R256 / -	Uni/Bipolar R263 / R264	R245 R258	R242 R260	R246 R257	C124 C131	C122 C130
J47	C	ADC2.B6	Shunt/Pull-down R273 R274 R275 / R518	Uni/Bipolar R285 / R286	R268 R277	R265 R283	R267 R276	C135 C144	C133 C141
J46	D	ADC2.B7	Shunt/Pull-down R278 R279 R280 / R517	Uni/Bipolar R287 / R288	R269 R282	R266 R284	R270 R281	C136 C143	C134 C142

Table 5: ADC's location on CDA01-CU5.

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Range	Order	Ra $[k\Omega]$	Rb $[k\Omega]$	Rc $[k\Omega]$	Ca $[nF]$	Cb $[nF]$
0V/+5V Unipolar	1st	3,3	2,2	0	NC	10
	2nd	33	22	13	3,3	1
0V/+10V Unipolar	1st	10	3,3	0	NC	10
	2nd	100	33	10	3,3	1
-5V/+5V Bipolar	1st	10	3,3	0	NC	10
	2nd	100	33	10	3,3	1
-10V/+10V Bipolar	1st	20	3,3	0	NC	10
	2nd	200	33	10	3,3	1

Table 6: ADC's configurations.

Analog inputs coming from external sensors can be connected to analog input connectors J40 to J55. These connectors are 2x2 connectors from Molex, manufacturer reference 39-29-0043. The header connectors that match J40-J55 are also from Molex, manufacturer reference 39-01-2040. The corresponding female crimping terminals are also from Molex, manufacturer reference 39-00-0090. Pin function of J40-J55 connectors is summarized in Table 7. Also, pin arrangement of J40-J55 connectors is shown in Figure 7.

Pin	Pin name	Function	Description
1	+15 V	Power	Power supply +15 V_{DC}
2	Measure	Signal	Analog signal input
3	-15 V	Power	Power supply -15 V_{DC}
4	GND	Power	Ground for power supply

Table 7: J40-J55 connector, pin function.

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Figure 7: J40-J55 connector, pin arrangement

2.8 Temperature Inputs

To compute the external temperature input magnitudes, a 5 $k\Omega$ NTC resistor must be connected to the corresponding connector (J31 to J35). The temperature-voltage curve can be calculated by solving electrically the circuit on figure 8 considering a NTC resistor in parallel with the 4,7 $k\Omega$ resistor depending on the NTC temperature.

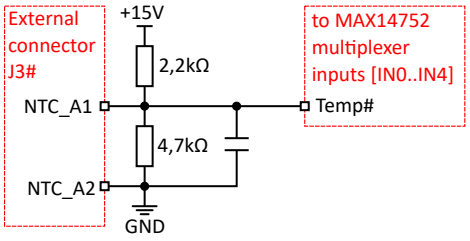


Figure 8: Temperature input schematics

As an example, the code below can be used for the B57550G0502+002 NTC resistor. The coefficients have been obtained from a 5 degree polynomial regression.

```
in = ((float) ADCRESULT) * 0.0009765625;
aux1 = 203.456136;
aux1 -= -189.448080*in;
aux2 = in*in;
aux1 += 127.449140*aux2;
aux2 = in*aux2;
aux1 -= 53.076494*aux2;
```


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```
aux2 = in*aux2;
aux1 += 11.457708*aux2;
aux2 = in*aux2;
aux1 -= 1.017662*aux2;
out = aux1;
```

Where:

1. *ADCRESULT* is the 12 bits ADC conversion result (range from 0 to 4095).
2. *in*, *aux1*, *aux2* are float type auxiliar variables.
3. *out* is the temperature value.

It is recommended to filter the temperatures with a low pass digital filter with time constant in the range of 1 to 5 s.

All temperature from external inputs and stack converters are passed through a multiplexer from Maxim Intergrated, manufacturer reference MAX14752. Pins GPIO131, GPIO132 and GPIO133 are used as selectors as indicated in Figure 9. Table 8 shows the pin configuration for output selection.

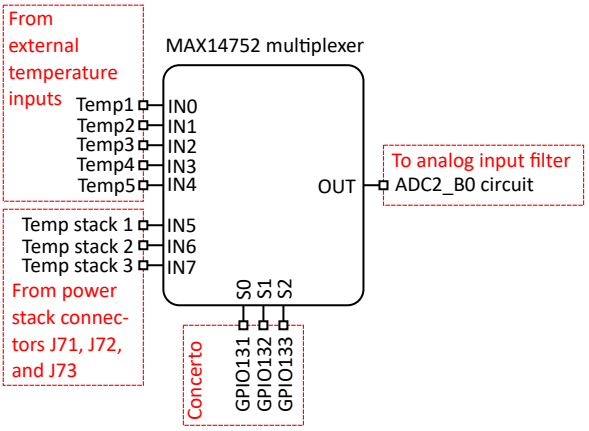


Figure 9: Temperature input multiplexer schematics

S2 (GPIO133)	S1 (GPIO132)	S0 (GPIO131)	Multiplexer Output
0	0	0	Temp1
0	0	1	Temp2
0	1	0	Temp3
0	1	1	Temp4
1	0	0	Temp5
1	0	1	Temp stack 1
1	1	0	Temp stack 2
1	1	1	Temp stack 3

Table 8: Multiplexer selector configuration

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J31-J35 are 1x2 connectors from Molex, manufacturer reference 39-29-0023. The header connectors that match J31-J35 are also from Molex, manufacturer reference 39-01-2020. The corresponding female crimping terminals are also from Molex, manufacturer reference 39-00-0090.

2.9 RS485

Non-isolated RS485 is available on board. ST3485 transceiver from ST is used. Moreover, two RJ45 connectors are available for the same channel. This makes possible chaining many devices on the RS485 communication bus.

The ST3485 transceiver pins to the Concerto microcontroller are shown in Figure 10 and listed in Table 9.

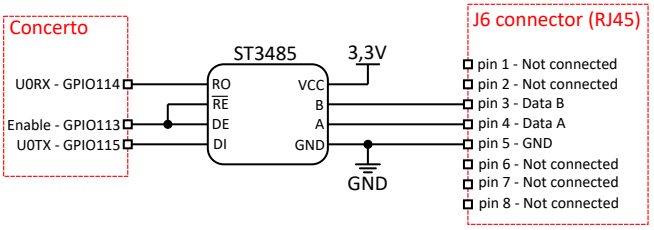


Figure 10: RS-485 schematics

ST3485 Pin	Concerto Pin
EN	GPIO113
RX	GPIO114
TX	GPIO115

Table 9: RS485, ST3485 transceiver pins

J6 connector is a double port standard RJ45, from Amphenol FCI, manufacturer reference 10118069-500A010LF. The pin-out of each RJ45 port is listed in Table 10.

Pin	Function	Description
RJ45 pin 1	NC	Not connected
RJ45 pin 2	NC	Not connected
RJ45 pin 3	Communication	RS485 data B
RJ45 pin 4	Communication	RS485 data A
RJ45 pin 5	Power	RS485 GND
RJ45 pin 6	NC	Not connected
RJ45 pin 7	NC	Not connected
RJ45 pin 8	NC	Not connected
RJ45 case	Case	Connected to Earth

Table 10: J6 connector, RS485 pin-out.

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2.10 Power Converter Interface

J71, J72 and J73 are the provided connectors for the power converter interface (also known as power stacks). The block diagram on Figure 11 shows how the Concerto microcontroller pins are linked to the connector pins. Although the pins can be used for several topologies, the pin out of J71, J72 and J73 is aimed to control the typical 3-phase 2-level voltage source converter with 3 IGBT or MOSFET transistor legs each with top and bottom transistor. The functionalities provided by each connector are as follows:

- 24 V supply for the control electronics in the power converter.
- 6 PWM signals for IGBT/MOSFET gate control (0-5 V).
- 1 extra PWM for cooling FAN control (0-5 V).
- Driver FAULT inputs, one for each leg (negative logic, 0-5V).
- A reset output for driver management (negative logic, 0-5 V open drain).
- ± 15 V with independent analog GND supply for the internal sensors of the power converter.
- 1 analog input for DC link voltage sensor (0…10 V range, only in J71).
- 2 analog input for 2 converter output currents (lines R and S, -5…5V voltage range).
- 1 analog input for the heat sink or temperature power module (0…10 V range).

The PWM signals voltage levels are shifted to 0-5 V with the SN74AHCT541 IC. The FAULT inputs are passed through RC low pas filters and Schmitt trigger buffers to suppress noise interference and drop the voltage level from 0-5V to 0-3,3V. The reset output is also shifted to 0-5 V but open drain output is provided in the connector pin. The temperature signal from the converter is connected to the multiplexer, as explained in section 2.8. Finally, the analog signal from the DC link voltage and current sensors in the power converter are wired to its ADC input. Pin arrangement detail and function of J71, J72 and J73 connectors are summarized in Table 11, Table 12 and Table 13 respectively.

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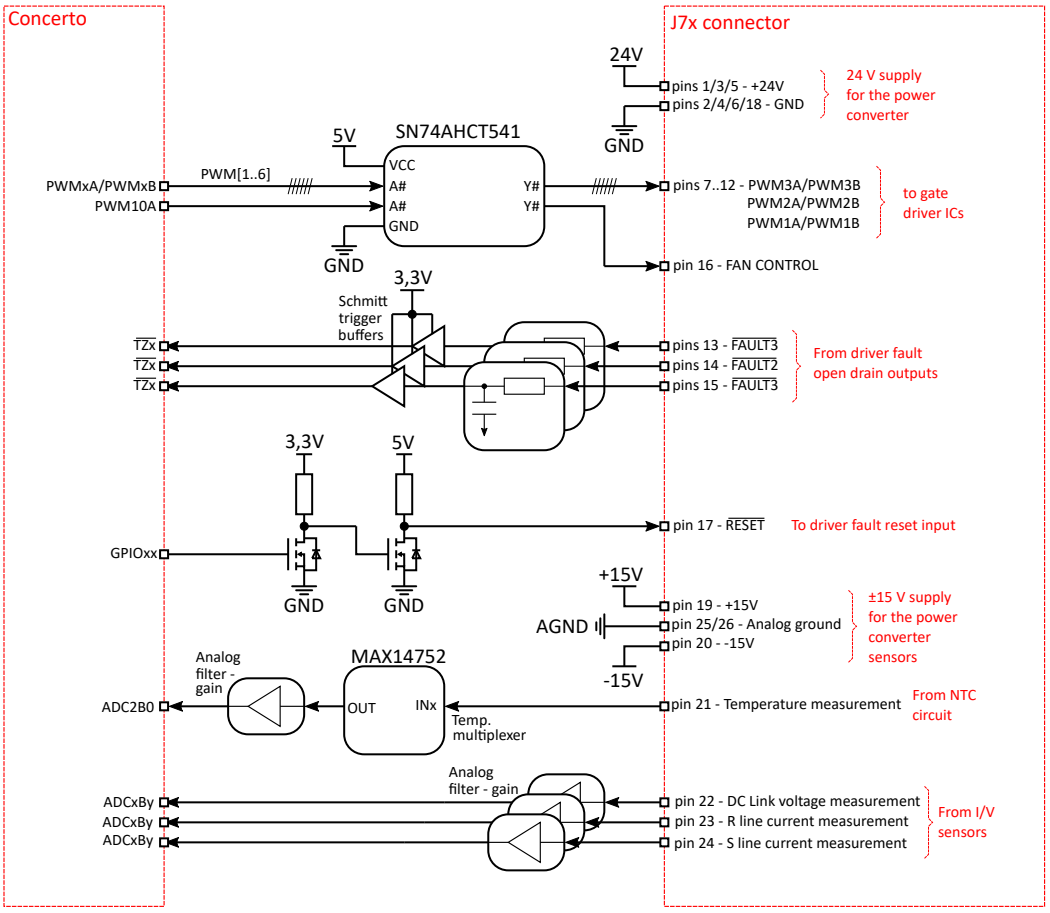


Figure 11: Power converter interface block diagram

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Pin	Pin name	Function	Description
1	24V drivers	Power	+24 V to supply the power stack
2	GND	Power	GND to supply the power stack
3	24V drivers	Power	+24 V to supply the power stack
4	GND	Power	GND to supply the power stack
5	24V drivers	Power	P+24 V to supply the power stack
6	GND	Power	GND to supply the power stack
7	PWM_3A	PWM Output	GPIO4, power transistor control
8	PWM_3B	PWM Output	GPIO5, power transistor control
9	PWM_2A	PWM Output	GPIO2, power transistor control
10	PWM_2B	PWM Output	GPIO3, power transistor control
11	PWM_1A	PWM Output	GPIO0, power transistor control
12	PWM_1B	PWM Output	GPIO1, power transistor control
13	FAULT3	PWM Input	GPIO23, driver FAULT 3
14	FAULT2	PWM Input	GPIO20, driver FAULT 2
15	FAULT1	PWM Input	GPIO30, driver FAULT 1
16	PWM_10A	PWM Output	GPIO130, control of the cooling fans of the stack
17	PWM_RESET	PWM Output	GPIO119, output for driver FAULT reset
18	GND	Power	GND to supply the power stack
19	+15V	Power	+15 V power to supply voltage/current sensors
20	-15V	Power	-15 V power to supply voltage/current sensors
21	Temp1	Analog Input	Temp stack 1 input (see section 2.8)
22	ADC2input.B4	Analog Input	ADC2.B4 analog input for DC link voltage measurement
23	ADC1input.A2	Analog Input	ADC1.A2 analog input for R line current measurement
24	ADC1input.B2	Analog Input	ADC1.B2 analog input for S line current measurement
25	AGND	Power	Analog Ground
26	AGND	Power	Analog Ground

Table 11: J71 connector, digital I/O interface, pin function and arrangement.

IMPORTANT NOTICE
GND and AGND must not be connected between each other.

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Pin	Pin name	Function	Description
1	24V drivers	Power	+24 V to supply the power stack
2	GND	Power	GND to supply the power stack
3	24V drivers	Power	+24 V to supply the power stack
4	GND	Power	GND to supply the power stack
5	24V drivers	Power	P+24 V to supply the power stack
6	GND	Power	GND to supply the power stack
7	PWM_6A	PWM Output	GPIO10, power transistor control
8	PWM_6B	PWM Output	GPIO11, power transistor control
9	PWM_5A	PWM Output	GPIO8, power transistor control
10	PWM_5B	PWM Output	GPIO9, power transistor control
11	PWM_4A	PWM Output	GPIO6, power transistor control
12	PWM_4B	PWM Output	GPIO7, power transistor control
13	FAULT6	PWM Input	GPIO14, driver FAULT 6
14	FAULT5	PWM Input	GPIO15, driver FAULT 5
15	FAULT4	PWM Input	GPIO31, driver FAULT 4
16	PWM_10A	PWM Output	GPIO130, control of the cooling fans of the stack
17	PWM_RESET	PWM Output	GPIO119, output for driver FAULT reset
18	GND	Power	GND to supply the power stack
19	+15V	Power	+15 V power to supply voltage/current sensors
20	-15V	Power	-15 V power to supply voltage/current sensors
21	Temp2	Analog Input	Temp stack 2 input (see section 2.8)
22	NC	NC	Not connected
23	ADC1input.A3	Analog Input	ADC1.A3 analog input for R line current measurement
24	ADC1input.B3	Analog Input	ADC1.B3 analog input for S line current measurement
25	AGND	Power	Analog Ground
26	AGND	Power	Analog Ground

Table 12: J72 connector, digital I/O interface, pin function and arrangement.

IMPORTANT NOTICE
GND and AGND must not be connected between each other.

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Pin	Pin name	Function	Description
1	24V drivers	Power	+24 V to supply the power stack
2	GND	Power	GND to supply the power stack
3	24V drivers	Power	+24 V to supply the power stack
4	GND	Power	GND to supply the power stack
5	24V drivers	Power	P+24 V to supply the power stack
6	GND	Power	GND to supply the power stack
7	PWM_9A	PWM Output	GPIO128, power transistor control
8	PWM_9B	PWM Output	GPIO129, power transistor control
9	PWM_8A	PWM Output	GPIO126, power transistor control
10	PWM_8B	PWM Output	GPIO127, power transistor control
11	PWM_7A	PWM Output	GPIO124, power transistor control
12	PWM_7B	PWM Output	GPIO125, power transistor control
13	FAULT9	PWM Input	GPIO32, driver FAULT 9
14	FAULT8	PWM Input	GPIO16, driver FAULT 8
15	FAULT7	PWM Input	GPIO17, driver FAULT 7
16	PWM_10A	PWM Output	GPIO130, control of the cooling fans of the stack
17	PWM_RESET	PWM Output	GPIO119, output for driver FAULT reset
18	GND	Power	GND to supply the power stack
19	+15V	Power	+15 V power to supply voltage/current sensors
20	-15V	Power	-15 V power to supply voltage/current sensors
21	Temp3	Analog Input	Temp stack 3 input (see section 2.8)
22	NC	NC	Not connected
23	ADC1input.A6	Analog Input	ADC1.A6 analog input for R line current measurement
24	ADC1input.B6	Analog Input	ADC1.B6 analog input for S line current measurement
25	AGND	Power	Analog Ground
26	AGND	Power	Analog Ground

Table 13: J73 connector, digital I/O interface, pin function and arrangement.

IMPORTANT NOTICE
GND and AGND must not be connected between each other.

J71, J72 and J73 are 13x2 connectors from HARTING, manufacturer reference 15120262601000. The female connectors that match J71, J72 and J73 connectors, reference 15290262502000, are also from HARTING.

2.11 DAC

DAC is implemented by TLV5614, a quadruple 12-bit voltage output digital-to-analog converter from Texas Instruments. 4 channels with 0 V – 4,095 V range are available. DAC is programmed by SPI of Cortex M3. The pins used for these communications are shown in Figure 12 and listed in Table 14.

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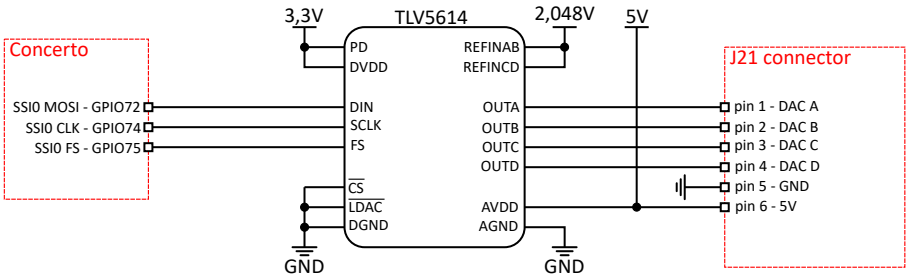


Figure 12: DAC connection

Function	Concerto Pin
SPI MOSI	GPIO72
SPI MISO	Not used - No Pin
SPI Clock	GPIO74
SPI Chip Select	GPIO75

Table 14: SPI communication pins

J21 connector is a 3x2 pin connector from Multicomp, manufacturer reference 2213S-6G. When this module is programmed, DAC output channels are available in this connector. Pin arrangement of J21 connector is shown in Figure 13 as viewed from the top of the CDA01-CU5. Table 15 illustrates the definition of J21, containing the DAC signals.

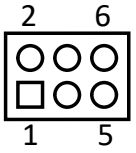


Figure 13: DAC connector J21 layout

Pin	Pin name	Function	Description
1	DAC A	Analog Output	DAC A channel
2	DAC B	Analog Output	DAC B channel
3	DAC C	Analog Output	DAC C channel
4	DAC D	Analog Output	DAC D channel
5	GND	Power	Ground
6	5V	Power	Power for DAC

Table 15: DAC connector J21 pin function and arrangement.

2.12 μUSB-OTG

The board supports USB On-The-Go (OTG), allowing it to function as either a host or a device.

J15 is a micro USB receptacle type AB connector from Tyco Electronics, reference 1981584-1. The definition of J15 is shown in Table 16.

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Pin	Pin name	Function	Description
1	VBUS	Power	5 V supply or supplied
2	D_N	Communication	Negative communication
3	D_P	Communication	Positive communication
4	PFLT	Communication	PFLT
5	GND	Power	Ground
6,7,8,9	EARTH	Case	EARTH

Table 16: J15 connector pin function and arrangement.

2.13 Ethernet

Ethernet is available on board. LAN8710A Ethernet transceiver from Microchip is used. Hardware design allows 10BASE-T/100BASE-TX of IEEE 802.3 support with speed up to 100 Mbps. LAN8710A transceiver pins to the Concerto microcontroller are listed in Table 17.

LAN8710A Pin	Pin name	Description	Concerto Pin
7	RX_CLK	Receive Clock (MII Mode)	GPIO95
8	RXD3	Receive Data 3	GPIO80
9	RXD2	Receive Data 2	GPIO81
10	RXD1	Receive Data 1	GPIO82
11	RXD0	Receive Data 0	GPIO83
13	RX_ER	Receive Error	GPIO94
14	CRS	Carrier Sense (MII Mode)	GPIO79
15	COL	Collision Detect (MII Mode)	GPIO65
16	MDIO	SMI Data Input/Output	GPIO88
17	MDC	SMI Clock	GPIO87
18	nINT	Interrupt Output	GPIO86
18	TX_ER	Transmit Error (MII Mode)	GPIO78
19	RESETn	External Reset	GPIO85
20	TX_CLK	Transmit Clock (MII Mode)	GPIO77
21	TX_EN	Transmit Enable	GPIO76
22	TXD0	Transmit Data 0	GPIO92
23	TXD1	Transmit Data 1	GPIO91
24	TXD2	Transmit Data 2 (MII Mode)	GPIO90
25	TXD3	Transmit Data 3 (MII Mode)	GPIO89
26	RX_DV	Receive Data Valid	GPIO93

Table 17: LAN8710A, concerto microcontroller pins.

J16 connector is a 100 Base-TX (Fast Ethernet) RJ45 1x1 Tab-DOWN with LEDs 8-pin (J0 series) Integrated Connector Modules (ICMs). The J16 connector is from Pulse Electronics, manufacturer reference J0011D01BNL. Definition of J16 is shown in Table 18.

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Pin	Pin name	Function	Description
1	TX_P	Communication	Transmit positive
2	TX_N	Communication	Transmit negative
3	RX_P	Communication	Receive positive
4	TXCT	Communication	Transmit
5	RXCT	Communication	Receive
6	RX_N	Communication	Receive positive
7	NC	-	Not connected
8,13,14	EARTH	Case	Earth
9	A_GREEN	Signalling	Anode green led
10	C_GREEN	Signalling	Cathode green led
11	C_YELLOW	Signalling	Cathode yellow led
12	A_YELLOW	Signalling	Anode yellow led

Table 18: Ethernet connector J16 pin function and arrangement

2.14 μSD

μSD is available on board, programmed by SSI3 of Cortex M3. The pins used for these communications are shown on Figure 14 and listed in Table 19.

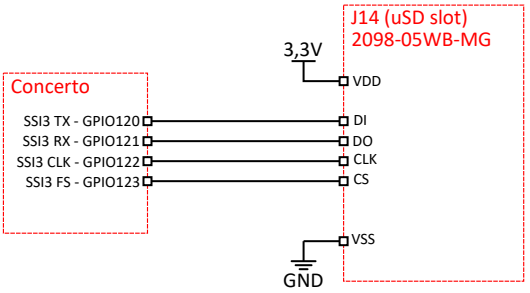


Figure 14: Micro SD card schematics

Function	Concerto Pin
SSI3-FSS	GPIO123
SSI3-TX	GPIO120
SSI3-CLK	GPIO122
SSI3-RX	GPIO121

Table 19: SSI communication pins

J14 is a standard polarization, push-push, surface mount, micro-SD connector. The J14 connector is from 3M, manufacturer reference 2908-05WB-MG. Definition of J14 is shown in Table 20.

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Pin	Pin name	Function	Description
1	NC	-	Not connected
2	FSS	Communication	Serial Frame
3	TX	Communication	Write
4	3,3 V μSD	Power	Power for μSD
5	CLK	Communication	Clock for communication
6,8	GND	Power	Ground
9,10,11,12	EARTH	Case	EARTH

Table 20: SD connector J14 pin function and arrangement

2.15 Temperature protection environment, RTC & EEPROM

The three modules communicate with the microcontroller through the I2C serial communication bus (I2C0 of Cortex M3), supporting a clock speed of up to 400 kHz. The pins used for these communications are listed in Table 21.

Function	Concerto Pin
SCL	GPIO96
SDA	GPIO97

Table 21: I2C communication pins

Temperature protection environment is implemented by DS75LXS from Analog Devices/Maxim Integrated, which provides up to 12-bit digital temperature readings over a -55°C to +125°C range. Its I2C address is 1001000. Real Time Clock is implemented by ISL1208 RTC from Intersil with an external 32,768 kHz quartz oscillator and a 1,5 F capacitor as a back-up battery. Its I2C address is 1101111. EEPROM is implemented by 24AA256UID of 256 kbits from Microchip and its I2C address is 1010001. These addresses are fixed by hardware. Connections from these elements to the Concerto microcontroller is shown in Figure 15

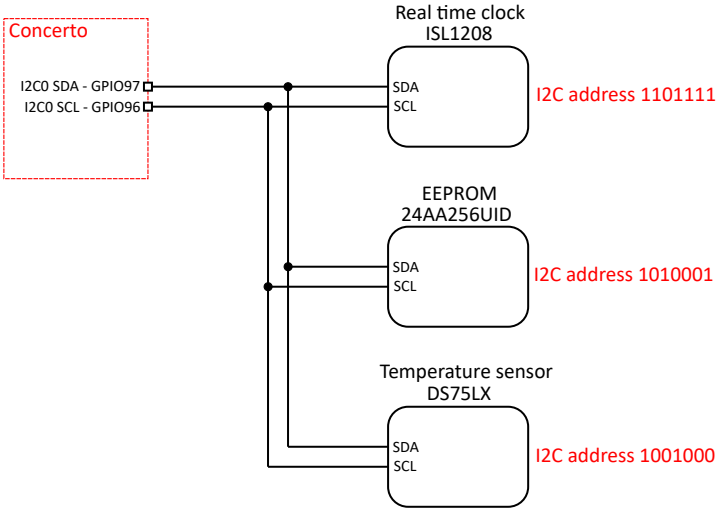


Figure 15: I2C communications schematics

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2.16 Fiber optic synchronization (F. O. SYNC.)

PWM synchronization can be helpful when connecting several converters on the same DC bus, but also is a requirement when implementing multilevel or interleaved topologies. PWM synchronization needs one input signal SYNC IN and one output signal SYNC OUT. In this control board, to avoid electromagnetic noise, fiber optic is used for this feature.

Concerto can work in two different modes, sending the PWM synchronization signal or receiving the PWM synchronization signal from another device. Figure 16 shows how to select the two possible configurations:

- Sending mode A: R532 is soldered and R533 is not soldered. In this mode, the Concerto microcontroller generates the PWM synchronization signal (SYNC OUT) as an output.
- Receiving mode B: R532 is not soldered and R533 is soldered. In this mode, the control board receives a PWM synchronization signal (SYNC OUT) sent by another device as input. This signal is resent to other device to be synchronized, also working in this same mode.

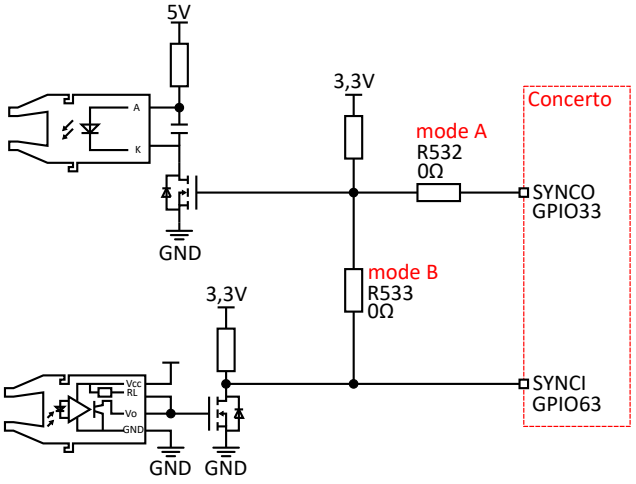


Figure 16: Fiber optic configuration schematics

IMPORTANT NOTICE
Only one of the mode A or mode B 0 Ω resistors can be soldered at the same time!

In order to be able to detect if SYNC In pulses are being received, a flip-flop is used to latch the high input state as shown in Figure 17. It can be checked if the SYNC IN pulse have been received at the beginning of each switching period interruption. In that case, the flip-flop should be cleared. In the same switching period routine, the flip-flop can be and preset through GPIO100 to allow the verification of the reception in the following interruption cycle. Table 22 shows the logic table of such feature.

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RST	SYNCIN	OUT
L	L	L
H	H	H
L	H	H (unstable)
H	L	OUT_0

Table 22: Flip flop logic table.

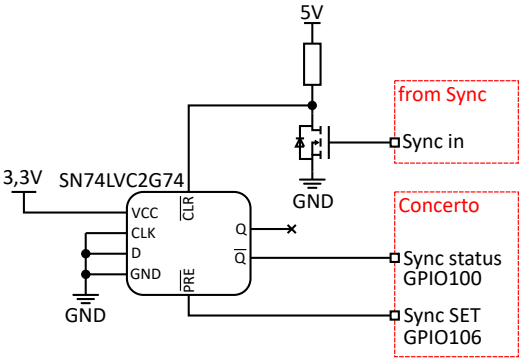


Figure 17: Flip-flop circuit schematics

The U16 connector is an optic fiber emitter from Avago, manufacturer reference HFBR-1521Z. The connector that matches the U16 is also from Avago, reference HFBR-4503Z.

The U17 connector is optic fiber receiver from Avago, manufacturer reference HFBR-2521Z. The connector that matches the U17 is also from Avago, reference HFBR-4503Z.

2.17 Isolated CAN

Isolated CAN is available on board. ISO1050 CAN transceiver from Texas Instruments and IE2405S DC/DC converter from XP Power are used. Furthermore, there is an end of line resistor of 120 Ω (R300) that has to be soldered or not, depending on the position of the device on the communication bus. Moreover, there are two RJ45 connectors for the same isolated channel, making it possible to chain many devices on the bus CAN communication. Figure 18 shows the CAN connections to the connector and to the Concerto microcontroller.

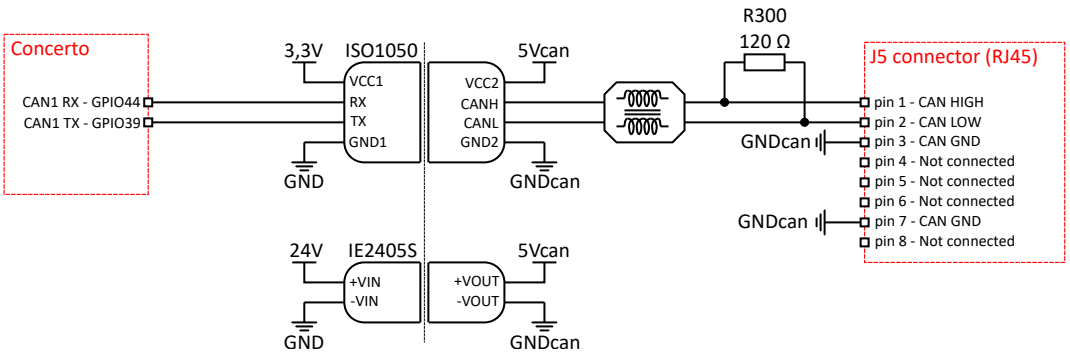


Figure 18: CAN circuit schematics

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J5 connector is a double port standard RJ45. The J5 connector is from FCI, manufacturer reference 10118069-500A010LF. The pin-out of J5 is shown in Table 23.

Pin	Pin name	Description
1	CAN H	CAN High
2	CAN L	CAN Low
3	CAN GND	CAN Ground
4	NC	Not connected
5	NC	Not connected
6	NC	Not connected
7	CAN GND	CAN GND
8	NC	Not connected

Table 23: CAN connector J5 pin function and arrangement

The CAN communication pins on the Concerto microcontroller are listed in Table 24.

Function	Concerto Pin
CAN RX	GPIO44
CAN TX	GPIO39

Table 24: CAN communication pins

2.18 Digital inputs

This module consists of 12 isolated digital inputs. The isolation is provided by ACPL-247 optoisolator from Avago. To energize these isolated inputs, IES0224S24 from XP power is used, which allows generating one external 24 V external power supply for all inputs.

0 Ω resistors are used to configure the digital inputs, either to detect the status of external devices potential-free contacts wired between A1 and A2 (R_up in Figure 19), or to detect 24V presence in the A1 pin (R_down in Figure 19). R_up or R_down resistors must be selected appropriately based on the input type.

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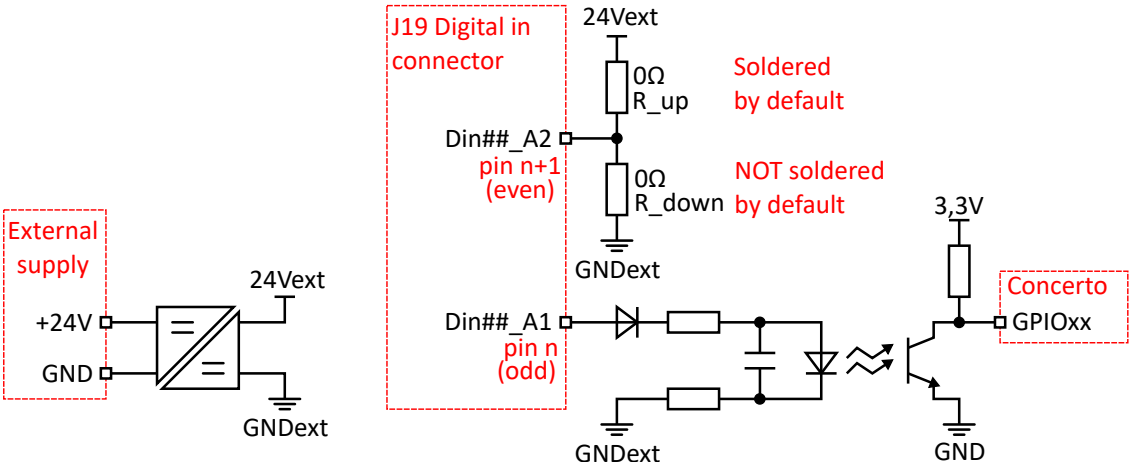


Figure 19: Digital inputs schematics

IMPORTANT NOTICE
For each digital input, only one of the two resistors, R_up or R_down, must be soldered. Be aware that digital inputs have negative logic.

J19 connector has 12x2 pin arrangement. 12 digital inputs are available in this connector. J19 is from Weidmuller, manufacturer reference 1290330000. The female connector that matches the J19 is also from Weidmuller, reference 1278340000. The female connector allows independent wiring of the wires, providing versatility for various applications. Pin arrangement and function of connector J12 is summarized in Table 25.

Input	pin A1	pin A2	R_up	R_down	GPIO
Din00	1	2	R411	R426	GPIO110
Din01	3	4	R410	R419	GPIO111
Din02	5	6	R409	R421	GPIO109
Din03	7	8	R408	R424	GPIO108
Din04	9	10	R406	R425	GPIO99
Din05	11	12	R405	R422	GPIO104
Din06	13	14	R404	R420	GPIO105
Din07	15	16	R403	R418	GPIO101
Din08	17	18	R401	R416	GPIO98
Din09	19	20	R400	R415	GPIO102
Din10	21	22	R399	R414	GPIO103
Din11	23	24	R398	R413	GPIO84

Table 25: Digital inputs pin configuration and arrangement

2.19 Relay outputs

Relay outputs are available on board. General purpose relays from TE connectivity are used, manufacturer reference PCN-124D3MHZ. Relay outputs are active high and the contacts are normally open (NO). Figure 20 shows the connection of each output.

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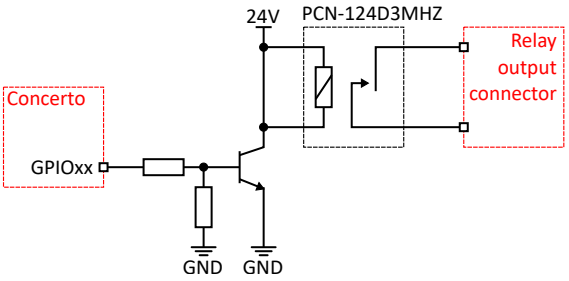


Figure 20: Relay outputs schematics

J1-J4, J7, J9, J17, J18, J20, J22-J28 are 16 relay output connectors from Molex, manufacturer reference 39-29-0023. The header connectors that match the relay output connectors are also from Molex, manufacturer reference 39-01-2020. The corresponding female crimping terminals are also from Molex, manufacturer reference 39-00-0090. Corresponding output and pins of the connectors is explained in Table 26.

Output	DSP pin	Connector
RLY00	GPO195	J1
RLY01	GPO117	J2
RLY02	GPO194	J3
RLY03	GPO116	J4
RLY04	GPO193	J7
RLY05	GPO192	J9
RLY06	GPO118	J17
RLY07	GPO112	J18
RLY08	GPO197	J20
RLY09	GPO196	J22
RLY10	GPO199	J23
RLY11	GPO198	J24
RLY12	GPO64	J25
RLY13	GPO66	J26
RLY14	GPO67	J27
RLY15	GPO73	J28

Table 26: Relay output connectors. J1-J4, J7, J9, J17, J18, J20, J22-J28 links to Concerto pins

2.20 Configuration by default of CDA01-CU5

2.20.1 Boot sequence

Boot from Flash is the CDA01-CU5 boot configuration by default. Figure 21 shows the soldered resistors.

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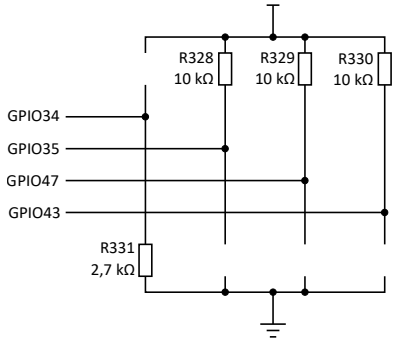


Figure 21: Boot configuration resistors by default.

2.20.2 ADC

Table 27 indicates configuration by default of ADCs, including Unipolar or Bipolar setting, measurement range, and the presence of pull-down resistors for voltage signals or shunt resistors for current signals.

Pin name	Description (ADC channel)	Unipolar/Bipolar	Range	Pull-down/Shunt
M	ADC1.A0	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
Stack 1 Ir	ADC1.B0	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
Stack 2 Ir	ADC1.A4	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
L	ADC1.A3	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
Stack 3 Ir	ADC1.B7	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
K	ADC1.B4	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
N	ADC1.A0	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
Stack 1 Is	ADC1.A2	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
Stack 2 Is	ADC1.A7	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
O	ADC2.A6	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
Stack 3 Ir	ADC2.A7	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
P	ADC2.A2	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
J	ADC2.A0	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
I	ADC2.B7	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
H	ADC2.B4	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
G	ADC2.B0	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
F	ADC1.A6	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
E	ADC2.B3	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
A	ADC2.A4	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
Temp[1..8]	ADC2.A3	Unipolar, 2nd order	0 V/+10V	100 $k\Omega$ Pull-down
Stack 1 V_{DC}	ADC2.B0	Unipolar, 2nd order	0 V/+10V	100 $k\Omega$ Pull-down
B	ADC1.A6	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
D	ADC2.B3	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt
C	ADC2.A4	Bipolar, 2nd order	-5V/+5V	16,63 Ω Shunt

Table 27: ADC's configuration by default.

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2.20.3 Digital input

All digital inputs have R_up soldered, so they are prepared to work with potential-free contacts.

2.20.4 Fiber optic synchronization

This module is configured as mode B.[1]

[1] Look Chapter 2.16 (it reads and sends simultaneously by default).

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2.21 Security Precautions

2.21.1 General precautions

Do not disconnect any cable while energized.

Do not pull any cable, which may cause their breaking or unplugging.

Before any intervention, ensure no voltage is still present on board and shut down any power supply connected to the CDA01-CU5.

2.21.2 Earthing

According to standard IEC 60439-1, the exposed conductive parts must be connected to the protective circuit using the appropriate connections.

All accessible metal parts (chassis connectors) should be grounded. CDA01-CU5 metal parts are designed to ensure earthing continuity. All metal chassis are connected to the spacers.

After mounting, the electrical resistance between earth and any accessible metal surface should be checked and measured to less than 3 mΩ.

For a correct earthing connection, the five spacers intended for earth connection (excluding HW5) must be connected to the earth cable.

Finally, five 100 pF 1000 V_{DC} capacitors (C163, C272, C273, C275 and C276) have been implemented closely to spacers HW2, HW4, HW3, HW6 and HW1 respectively. These capacitors connect GND and EARTH, as providing a good path for electromagnetic noise generated is desired. These capacitors are from Multicomp, manufacturer reference MC1206B102K102CT.

IMPORTANT NOTICE
HW5 must not be connected to GND, as it is placed in the analog side of the PCB.

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3 Layout

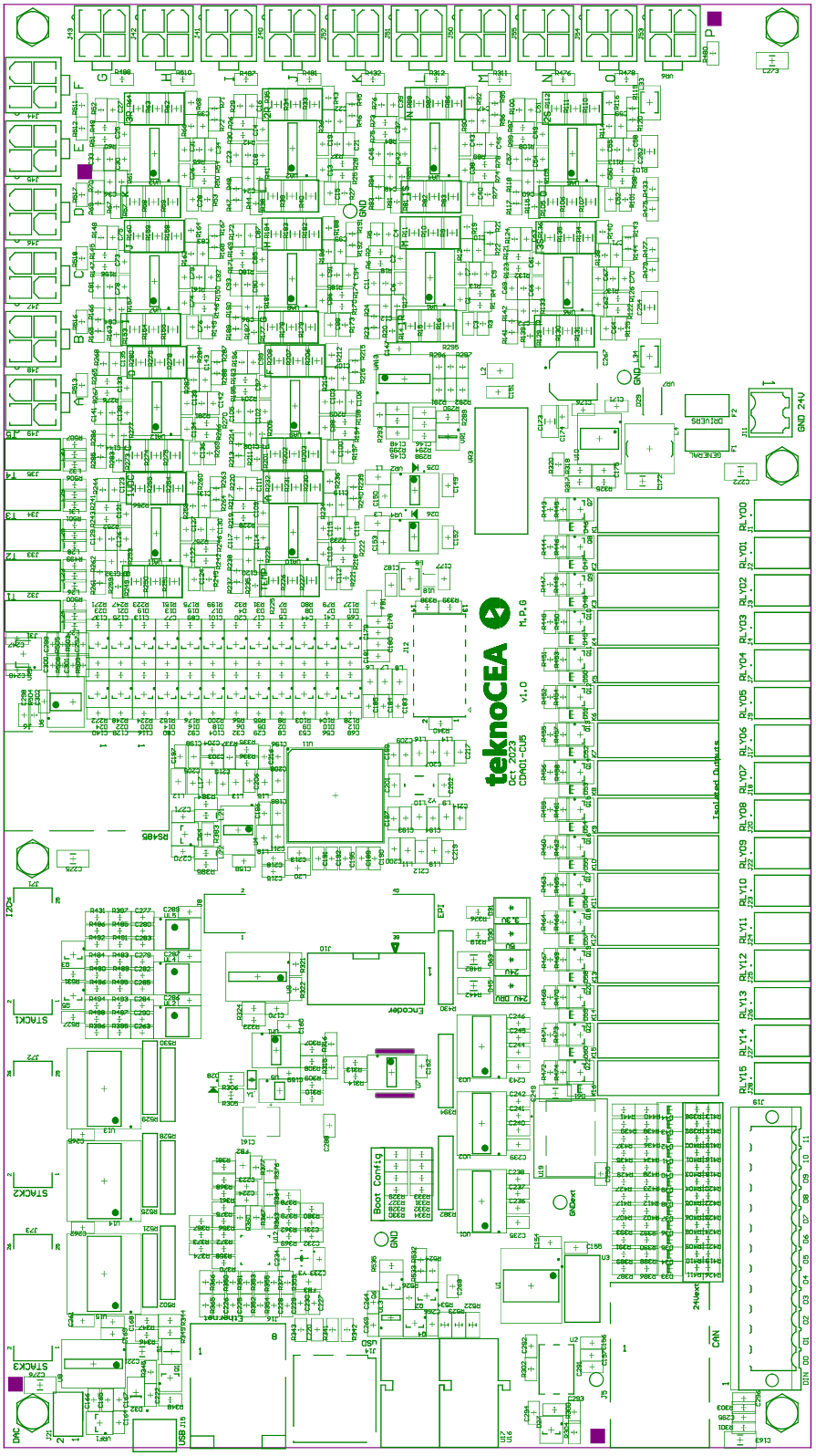


Figure 22: CDA01-CU5 Layout.

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4 Mechanical drawings

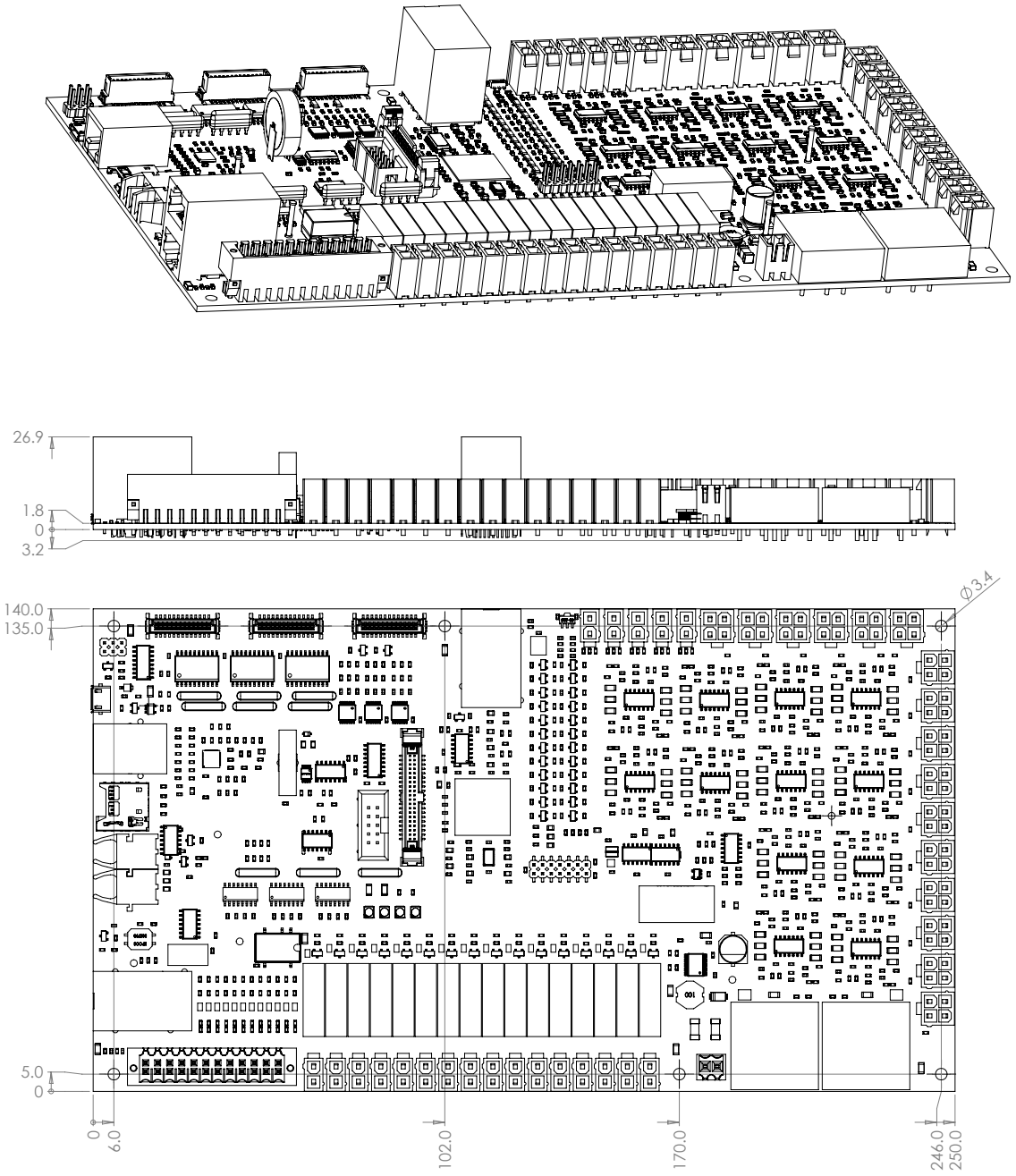


Figure 23: CDA01-CU5 Mechanical drawings.

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